

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A device, comprising:

a voltage level detector comprising an NMOS tail current transistor; and

a voltage generator coupled to a gate of the tail current transistor;

wherein the voltage generator is configured to deliver a voltage to the gate of the tail current transistor;

wherein a first component of the voltage is approximately equal to ~~the~~ a threshold voltage (V_t) of NMOS transistors comprised in the device; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature ~~as well as~~ and/or variations in transistor fabrication parameters;

2. (Currently Amended) The device of claim 1, wherein the voltage generator comprises a diode-connected NMOS transistor and a constant current sink configured to produce the first component of the voltage;

wherein ~~the~~ a source of the diode-connected ~~NMOS~~ transistor is coupled to ~~the~~ an input of ~~a~~ the constant current sink;

wherein ~~the~~ an output of the constant current sink is coupled to a negative supply;

~~wherein in the channel geometry of the transistor, W/L , and the current drawn by the current sink, I , are such that $(I/\beta)^{1/2} \ll V_t$, the NMOS threshold voltage;~~

~~wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current (I) drawn by the constant current sink, satisfies $(I/\beta)^2 \ll V_t$; and~~

~~wherein the first component of the voltage is produced as the a gate-source voltage of the diode-connected NMOS-transistor;~~

3. (Currently Amended) The device of claim ~~1~~2, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.

4. (Currently Amended) The device of claim ~~1~~3, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce ~~the a~~ sum of the first and second components of the voltage at ~~the a~~ gate of the diode-connected NMOS-transistor;

~~wherein the an~~ output of the bandgap voltage reference is coupled to ~~the an~~ inverting (negative) input of the amplifier;

~~wherein the source of the diode-connected NMOS-transistor is coupled to the non-~~ inverting (positive) input of the amplifier;

~~wherein the an~~ output of the amplifier is coupled to ~~the a~~ gate of the PMOS transistor;

~~wherein the a~~ drain of the PMOS transistor is coupled to the gate and drain of the diode-connected NMOS-transistor; and

wherein ~~the~~ a source of the PMOS transistor is coupled to a positive supply.

5. (Currently Amended) The device of claim 1, wherein the first component of the voltage provides ~~the~~ a threshold-minimum voltage required to turn on the tail current transistor, ~~despite~~ substantially unaffected by variations in operating temperature ~~as well as variations~~ and/or variations in transistor fabrication parameters.

6. (Currently Amended) The device of claim 1, wherein the second component of the voltage provides a constant effective voltage, ~~—~~ (Veff), for the tail current transistor, ~~which produces the tail current transistor thereby producing the tail current, —~~ (It, —) proportional to ~~beta of the NMOS process~~ an NMOS process beta parameter according to ~~the relationship:~~
$$I_t = (\beta/2) \cdot (V_{eff})^2$$

7. (Currently Amended) The device of claim 1, further comprising a differential pair of NMOS transistors whose emitters are coupled to ~~the~~ a drain of the tail current transistor, ~~and in which the~~ wherein a channel-width-to-length-ratio-channel-width-to-length ratio of the ~~a first transistor~~ one of the differential pair of NMOS transistors differs from ~~that of the~~ a —channel-width-to-length ratio of the ~~second one of the differential pair of NMOS transistors.~~

8. (Currently Amended) The device of claim 1, wherein ~~the~~ a trip point of the voltage level detector is ~~approximately~~ substantially constant despite variations in operating temperature as well as variations in transistor fabrication parameters.

9. (Currently Amended) A device, ~~—~~ comprising:

a differential amplifier comprising an NMOS tail current transistor; and

a voltage generator coupled to a gate of the tail current transistor;

wherein the voltage generator is configured to deliver a voltage to the gate of the tail current transistor;

wherein a first component of the voltage is approximately equal to ~~the~~ a threshold voltage (V_t) of NMOS transistors comprised in the device over variations in operating temperature as well as variations in transistor fabrication parameters; and

wherein a second component of the voltage is approximately constant with respect to variations in operating temperature ~~as well as~~ and/or variations in transistor fabrication parameters;

10. (Currently Amended) The device of claim 9, wherein the voltage generator comprises a diode-connected NMOS transistor and a constant current sink configured to produce the first component of the voltage;

wherein ~~the~~ a source of the diode-connected NMOS-transistor is coupled to ~~the~~ an input of ~~a~~ the constant current sink;

wherein ~~the~~ an output of the constant current sink is coupled to a negative supply;

~~wherein in the channel geometry of the transistor, W/L , and the current drawn by the current sink, I , are such that $(I/\beta)^{1/2} \ll V_t$, the NMOS threshold voltage;~~

wherein a configuration of channel-width-to-length ratio (W/L) of the diode-connected transistor, in conjunction with a current (I) drawn by the constant current sink, satisfies $(I/\beta)^{1/2} \ll V_t$; and

wherein the first component of the voltage is produced as ~~the~~ a gate-source voltage of the diode-connected NMOS-transistor;

11. (Currently Amended) The device of claim 910, wherein the voltage generator further comprises a bandgap voltage reference configured to produce the second component of the voltage as its output.

12. (Currently Amended) The device of claim 911, wherein the voltage generator further comprises an amplifier and a PMOS transistor configured to produce ~~the~~ a sum of the first and second components of the voltage at ~~the~~ a gate of the diode-connected NMOS-transistor;

wherein ~~the~~ an output of the bandgap voltage reference is coupled to ~~the~~ a negative (inverting) input of the amplifier;

wherein the source of the diode-connected NMOS-transistor is coupled to the positive (non-inverting) input of the amplifier;

wherein ~~the~~ an output of the amplifier is coupled to ~~the~~ a gate of the PMOS transistor;

wherein ~~the~~ a drain of the PMOS transistor is coupled to the gate and drain of the diode-connected NMOS-transistor; and

wherein ~~the~~ a source of the PMOS transistor is coupled to a positive supply.

13. (Currently Amended) The device of claim 9, wherein the first component of the voltage provides ~~the~~ a threshold-minimum voltage required to turn on the tail current transistor, ~~despite~~ substantially unaffected by variations in operating temperature ~~as well as variations~~ and/or variations in transistor fabrication parameters.

14. (Currently Amended) The device of claim 9, wherein the second component of the voltage provides a constant effective voltage, (V_{eff}), for the tail current transistor, ~~which produces~~ the tail current transistor thereby producing the tail current;

(It), proportional to ~~beta of the NMOS process~~an NMOS process beta parameter according to the relationship: $I_t = (\beta/2) \cdot (V_{eff})^2$.

15. (Currently Amended) The device of claim 9, wherein ~~the an~~ offset voltage of the differential amplifier is ~~approximately constant despite~~ substantially unaffected by variations in operating temperature ~~as well as~~and/or variations in transistor fabrication parameters, thereby remaining substantially constant.

16. (Currently Amended) A method comprising:

generating a constant reference voltage;

generating a threshold voltage component, wherein a the threshold voltage that component approximates the a threshold voltage of an NMOS process over variations in operating temperature as well asand variations in transistor fabrication parameters; ~~and~~

generating a composite voltage that is ~~the a~~ sum of the constant reference voltage and the voltage that approximates the threshold voltage of the NMOS processthreshold voltage component; and

applying the composite voltage to a gate of a tail current transistor of a voltage level detector, thereby producing a trip point of the voltage level detector that is substantially independent of operating temperature and/or variations in transistor fabrication parameters, the trip point thereby remaining substantially constant.

17. (Cancelled)

18. (Currently Amended) The method of claim ~~17~~16, wherein the threshold voltage component of the composite voltage turns on the tail current transistor despite

variations in operating temperature ~~as well as~~and/or variations in transistor fabrication parameters.

19. (Currently Amended) The method of claim 18, wherein the constant reference voltage component of the composite voltage produces a tail current for the voltage level detector that is proportional to a beta for the NMOS process.

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)

24. (Cancelled)

25. (New) The method of claim 16, wherein the voltage level detector is a differential amplifier.

26. (New) The method of claim 25, wherein an offset voltage of the differential amplifier remains substantially constant despite variations in operating temperature and/or variations in transistor fabrication parameters.